

CLAIMS

What is claimed is:

1. A method for evaluating gate timing in an integrated circuit (IC) design, said method comprising:

determining when a first-type of signal is present on an input to a logical gating device, wherein said first-type of input signal inhibits transitions on an output of said gating device;

determining when a second-type of signal is present on said input, wherein said second-type of input signal allows transitions on said output of said gating device; and

modifying a timing of a sensing of said first-type of signal to sense said first-type of signal at an earlier point in time than said second-type of signal is sensed.

2. The method of claim 1, wherein:

said input comprises a gate input;

said first-type of signal and said second-type of signal comprise gating signals; and

said first-type of signal and said second-type of signal control whether pulses on a clock input of said logical gating device are propagated to said output of said gate device.

- 1 3. The method of claim 1, wherein:
- 2 said input comprises a clock input;
- 3 said first-type of signal and said second-type of signal comprise clock trailing edge
- 4 signals;
- 5 said first-type of signal prevents a transition at said output of said gate device due to a
- 6 transition on a gate input of said gate device; and
- 7 said second-type of signal causes a transition at said output of said gate device.
- 10
- 11 4. The method of claim 2, wherein said first-type of signal prevents said clock pulses from
- 12 being propagated on said output of said gating device and said second-type of signal allows said
- 13 clock pulses to be propagated on said output of said gating device.
- 14
- 15 5. The method of claim 2, wherein said sensing time is used in computing a setup test.
- 16
- 17 6. The method of claim 3, wherein said sensing time is used in computing a hold test.
- 18
- 19 7. The method in claim 2, wherein said modifying prevents a delay in propagation of said
- 20 gate signal across said gating device from inappropriately reporting the outputting a portion of a
- 21 clock pulse.

1 8. The method of claim 1, wherein said modifying includes assuming there is no load on
2 said output.

1 9. The method in claim 1, wherein said modifying includes identifying a beginning point of
2 a transition of said first-type of signal as said sensing time.

1 10. The method of claim 4, wherein the computing of said setup test comprises:
2 computing a conventional propagated mode test value.
3 computing an input-to-input test value of zero, and
4 using the less pessimistic of said computed test values.

1 11. A method for evaluating gate timing in an integrated circuit (IC) design, said method
comprising:

2 determining when a first-type of signal is present on an input to a logical gating device,
3 wherein said first-type of input signal inhibits a clock pulse from being output from said gating
4 device;

5 determining when a second-type of signal is present on said input, wherein said
6 second-type of input signal allows said clock pulse to be output from said gating device; and
7 modifying a timing of a sensing of said first-type of signal to sense said first-type of
8 signal at an earlier point in time than said second-type of signal is sensed.

1 12. The method of claim 11, wherein:
2 said input comprises a gate input;
3 said first-type of signal and said second-type of signal comprise gating signals.

1 13. The method of claim 11, further comprising performing a hold test between said input
2 and a clock input of said gating device.

1 14. The method in claim 11, wherein said modifying prevents a delay in propagation of said
2 gate signal across said gating device from inappropriately reporting the outputting a portion of
3 said clock pulse.

1 15. The method of claim 11, wherein said modifying includes assuming there is no load on
2 said output.

1 16. The method in claim 11, wherein said modifying includes identifying a beginning point of
2 a transition of said input toward said first-type of signal as said sensing time of said first-type of
3 signal.

1 17. A program storage device readable by machine, tangibly embodying a program of
2 instructions executable by said machine for performing a method of evaluating gate timing in an
3 integrated circuit (IC) design, said method comprising:

4 determining when a first-type of signal is present on an input to a logical gating device;

5 wherein said first-type of input signal inhibits transitions on an output of said gating device;

6 determining when a second-type of signal is present on said input, wherein said

7 second-type of input signal allows transitions on said output of said gating device; and

8 modifying a timing of a sensing of said first-type of signal to sense said first-type of

9 signal at an earlier point in time than said second-type of signal is sensed.

1 18. The program storage device of claim 17, wherein:

2 said input comprises a gate input;

3 said first-type of signal and said second-type of signal comprise gating signals; and

4 said first-type of signal and said second-type of signal control whether pulses on a clock

5 input of said logical gating device are propagated to said output of said gate device.

1 19. The program storage device of claim 18, wherein said first-type of signal prevents said

2 clock pulses from being propagated on said output of said gating device and said second-type of

3 signal allows said clock pulses to be propagated on said output of said gating device.

1 20. The program storage device of claim 18, further comprising performing a hold test

2 between said input and said clock input of said gating device.

1 21. The program storage device in claim 18, wherein said modifying prevents a delay in
2 propagation of said gate signal across said gating device from inappropriately reporting the
3 outputting a portion of a clock pulse.

1 22. The program storage device of claim 17, wherein said modifying includes assuming there
2 is no load on said output.

1 23. The program storage device in claim 17, wherein said modifying includes identifying a
2 beginning point of a transition of said input toward said first-type of signal as said sensing time
3 of said first-type of signal.